REMARKS/ARGUMENTS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

The Examiner rejects to the title of the invention as not being descriptive. The title was changed to "Security System for Integrated Circuit Computer System" although apparently the older title was utilized in the appeal brief. The Examiner suggests the title of "Utilizing Password Registers to Block Scanned-Path Access" because he states that scanned-port access/denial through the use of registers and passwords is central to that which applicant regards as the invention.

Applicants have changed the title to "Security System for Scan-Path Access". Applicants do not agree that the use of registers is required, as the recitation of registers to control the scan-path access does not appear in the independent claims.

The Examiner objects to Claims 5-7, 10-13 and 15-17 under 35 C.F.R. 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim. The Examiner states that Claims 5, 10 and 15 recite that a plurality of commands are applied in a specific time sequence. The Examiner states that it is inherent that a plurality of commands which are applied are applied in a specific time sequence.

This objection is respectfully traversed. As is well know to those in the computer art, computer systems have an input labeled "interrupt" which is utilized specifically for the receipt of commands which are not in a specific time sequence. Therefore, it is well known to those skilled in the art that commands to a computer system can be applied in sequence in which there is a specific time sequence or out of sequence in which no time sequence exists. Accordingly, the recitation of that the plurality of commands are

applied in a specific time sequence does further limit applicant's invention and are appropriate dependent claims.

The Examiner states that Claims 6, 7, 11-13 and 16-17 also recite a comparator. The Examiner states that the respective independent claims recite "comparing" and that is inherent that a comparator would be required to carry out such a comparison.

This objection is respectfully traversed. A comparator is a specific electronic circuit utilized for comparing two signals. However, as is well known to those skilled in the art, comparisons can also be done within a computer system within the CPU, and thus the utilization of a specific circuit "comparator" is not required. In addition, these claims all additionally recite that the computer system further comprises a pair of registers and that the comparators are coupled to compare the contents of the registers. As such, these claims add additional structure to the independent claims and specifically recite that it is the contents of the two registers, which are not recited in the independent claims, that are coupled to a comparator. Accordingly, applicants believe that these are appropriate dependent claims.

The Examiner rejects 4-21 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or to which it is most nearly connected, to make and/or use the invention. The Examiner also rejects these claims under 35 U.S.C. 112, first paragraph, as containing subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application, was filed had possession of the claimed invention.

Taking the second rejection first, applicants have carefully reviewed the first paragraph of 35 U.S.C. 112, and find no requirement that the invention's convey to one skilled in the art that they had possession of the claimed invention. Nor has the

Examiner cited any case law for this proposition. However, applicants believe that the discussion below will overcome this rejection.

With respect to the first '112, first paragraph rejection, enclosed herewith is a Declaration under 37 C.F.R. 1.132 of Yasuhiro Ikeyoshi. Mr. Ikeyoshi had no knowledge of the present invention when he was asked to read the present application and solely utilizing the information therein generate a computer program for performing the password function. According to his declaration, this process took about one hour. Even if debugging of the computer program is required, he believes that it can readily be made to perform the task utilizing routine measures. Accordingly, applicants submit that if one of ordinary skill in the art could read the application and prepare an appropriate computer program to perform the password function within about an hour, that the specification certainly enables one skilled in the art to which it pertains to make and/or use the invention. This would also indicate that the inventor "had possession of the invention" at the time the application was filed, or else he could not describe it in sufficient manner to enable one skilled in the art to prepare this computer program in a relatively short period of time. Clearly no undue experimentation was involved.

Accordingly, applicants request that both of the Examiner's rejections under 35 U.S.C. 112, first paragraph, be withdrawn.

The Examiner rejects Claims 8, 10 and 14-15 under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounted to a gap between the steps. The Examiner also rejects the same claims under 35 U.S.C. 112, second paragraph as being incomplete for omitting essential structural co-operative relationships of elements, such omission amounting to a gap between the necessary structural connections. The Examiner states that there is insufficient detail describing the relationship between the input ports, the processor and the program and how the password is actually generated with respect to the first rejection, and insufficient detail describing the relationship between the input ports, the processor and the program regarding the second rejection. The Examiner specifically refers to MPEP

section 2172.01. In paragraph 51 of the rejection, entitled "Response to arguments - 112 rejections", the Examiner states "that applicants arguments relating to system and method claims are noted but not persuasive.". The Examiner has provided no further elucidation of his rejections.

MPEP 217.01 recites, in a relative portion "such essential matter may include missing elements, steps or necessary structural co-operative relationships of elements...". However, this does not mean that the same claim should include both missing co-operative relationships of elements and missing steps. It is clear that method steps do not belong in device claims and that device elements do not belong in method claims. The Examiner has not rejected any of these claims as containing inappropriate methods limitations in device claims or vice versa. Applicants have previously stated for the record that the claims rejected by the Examiner are not method claims but are device claims. Accordingly, the MPEP may utilize a single section relating to a problem with either method or device claims, that does not authorize the Examiner to make a rejection which requires the addition of method steps into device claims. Accordingly, the Examiner's rejection of these device claims as omitting essential step, should be withdrawn as being inappropriate to device claims.

With respect to the Examiner's rejection as omitting essential co-operative relationships to the elements, applicants readily believe that the claims as currently formulated provide adequate description of the functional relationship between the elements. However, in view of the long prosecution of this application, Applicants have amended Claims 8, 9 and 14, 15 in order to more clearly recite the structural co-operative relationships between the elements. In Claim 8, the scan-path interface circuit, which was not coupled to other elements of the claims has been removed in order to overcome the Examiner's objection to lack of co-operative relationships and has been moved to be initially recited in Claim 9 where such co-operative relationships are better described.

The Examiner rejects Claims 8, 11 and 13 as having insufficient antecedent basis for the term "said switching circuit".

Claim 8 is an independent claim and therefore does not have a problem with respect to a claim on which it is dependent and furthermore does not recite the phrase "said switching circuit". Accordingly, Applicants traverse the Examiner's requirement with respect to Claim 8. However, with respect to Claims 11 and 13, the Examiner is correct in that there is currently no antecedent basis for these term "said" and it has therefore been replaced with --a-- in both claims.

The Examiner rejects Claims 14 and 15 under U.S.C. 102(b) as being clearly being anticipated by Palmer, Jr. et al. The Examiner states that this reference shows applying a plurality of commands to a plurality of ports for a processor of the system as specifically refers to item 6a, the block labeled process control program, item 4 and item 6f, as well as to a program stored in memory coupled to the processor for operating the processor to process the plurality of commands to produce a password and this refers to Figure 2 item 6i, 6c, and comparing the produced password with a predetermined password.

This rejection is respectfully traversed. First of all, it should be pointed out that item 6f is an appliance access control, which is an output port of the device. As is well known to those skilled in the art, commands are not applied to an output port of the processor, commands to the processor can only be applied to an input port thereof.

More importantly, the Examiner refers to item 6c in this rejection and in a further rejection based on this reference in paragraph 20 of the official action, the Examiner refers to items 4 and 6c. These items are the card reader 4 and the card reader portion of the access control module 6, respectively. Referring now to Figure 2 of the cited reference, the optical card reader 6c is coupled to the single chip microcomputer 6i via a clock line and a data line which forms a first port. The password entered via the optical card reader is compared with a password stored in the ROM of the single chip

microcomputer, which is interal to the microcomputer, as clearly shown in Figure 2. Accordingly, applying this reference to the present invention, the "command" would be applied to the port T0, T1; would be read by the single chip microcomputer and compared to a password stored in its memory. There is no showing of the password being generated by a plurality of commands applied to a plurality of ports for the processor. Just to make sure that the concept of "port" is clear, applicants submitted with the appeal brief a portion of the text "Imbedded Microprocessor Systems - Real World Design" by Stuart R. Ball and incorporate that definition in this response. Furthermore, applicants enclose herewith a copy of a portion of the text "Programming Embedded Systems I" by Michael J. Paunt which clearly shows on page 1-12 that standard 8051s (microprocessors) have four 8-bit ports, all the ports being bidirectional. Therefore, it should be clear that a "port" is a group of I/O pins on a microcomputer chip which operate together for a particular function.

Thus, the fact that the store computer system inputs a "seed" into the access control module of the cited reference is irrelevant here because the seed and the clock output are used to find the password stored in the computer which is compared to the input password. Therefore, even if one were to ignore the arguments above and characterize the seed as a second command, it would not anticipate the present invention or render it obvious because it is not used to generate the password, which is read by the optical card reader. Although the Examiner has not specifically discussed the possibility, even if one were to reverse the situation in which the seed were read in through the optical card reader and the password came in through the main computer interface port, the situation would not change, because the information coming through the main computer interface port is a "seed" which is combined with an output of the clock to produce a pointer to the password. The hardware system clock and software clock are both shown in Figure 2 as being internal to the single chip microcomputer 6i and thus do not come from a second port.

In view of the fact that the claim recites applying a plurality of commands to a plurality of ports and having the program operating the processor or being operable to

control the processor to process the plurality of commands to produce a password, Claim 14 is clearly distinguished from this reference. Claim 15 is dependent upon Claim 14 and is therefore distinguished over the reference for the same reasons.

The Examiner rejects Claims 14-15 under 35 U.S.C. 102(e) as being clearly anticipated by Angelo. The Examiner states that Angelo discloses a method for enabling power to all portions of a computer system based upon the results of a two-piece user verification process as complete as part of a secure power-up procedure. The Examiner specifically highlights portions of the text including at some point during the secure power-up procedure, the computer user provides an external token or smart card that is coupled to the computer using specialized hardware and that the computer user is required to enter a plain text user password or, a password generated by the aid of biometrics.

This rejection is respectfully traversed. First of all, the Angelo reference is not to an integrated circuit computer system, as required by Claim 14. The system described in Angelo at col. 3, lines 48-58 includes bay door/case locks and mass data storage devices. The system provides security by withholding power to the peripheral devices and to the bay door/case locks forcing the possessor of a stolen computer to physically damage the computer casing. Accordingly, this reference is not applicable to the present invention, where such devices can not exist. Furthermore, a '102 rejection requires all elements of the claim to be present, which is clearly not true here. Moreover, the two-piece nature of the authorization process, does not require utilization of two input ports on a processor. In fact, referring to Figure 1, we see that the keyboard controller 136 has coupled thereto a keyboard 159 via keyboard connector 158 and a probe 186, into which the token 188 is plugged, is coupled via an RS-232 connector 146 and a com port adapter 184. Accordingly, both of the inputs into the system that are required, that is, the token and the typed in password, pass through the floppy controller 136 and via a single bus into the port comprising lines 106 and 108. Therefore, this reference fails to show or suggest the application of a plurality of

commands to a plurality of ports for generating a password, as required in Claim 14. Claim 15 is dependent upon Claim 14 and is therefore patentable for the same reasons.

The Examiner rejects Claims 4, 5, 8, 9, 10 and 15 under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al in view of Raghavavhari. The Examiner states that Palmer, Jr. et al does not expressly disclose a scan-path interface circuit for reading out a predetermined memory or register in the system and that this is disclosed in Raghavavhari. The Examiner concludes that it would have been obvious to one of ordinary skill in art at the time the invention was made to combine the two references.

This rejection is respectfully traversed. First of all, the discussion above concerning Palmer, Jr. et al applies here and Claim 4 clearly requires a plurality of commands applied to a plurality of input ports on a processor to process the commands to produce a password, which is not shown by Palmer, Jr. et al.

Furthermore, with regards to Raghavavhari, Figure 1 clearly shows that all input to the system comes through the port comprising lines TCK, TMS and TDI. These lines come through the boundary scan-port and control 15. No other input lines are shown. Therefore, these lines comprise the only input port to the device. Accordingly, this reference can not show or suggest the application of a plurality of commands to a plurality of input ports and processed to generate a password, as required by Claim 4. In fact, since both references show the utilization of a single port, the combination teaches away from the present invention.

Claim 5 is dependent upon Claim 4 and is therefore patentable for the same reasons.

With respect to Claim 8, the Examiner specifically points to the direction of the arrows of the process control program in Palmer, Jr. et al. However, Claim 8 recites that the processor receives a plurality of commands applied to a plurality of input ports and processed to produce a password. The fact that there are two inputs to the process

control program, is not dispositive because reading the text of the application clearly shows that the card reader 4, 6c is used to input the password and the access control module 2 and main computer interface 6a are used to input a parameter which is used to select the predetermined word against which the password is compared. Thus, the inputs through both ports are not utilized to generate the password. Thus, as discussed above, the present invention is clearly distinguished from Palmer, Jr. et al.

The Examiner states that with regard to Claim 9, Palmer, Jr. et al does not expressly disclose a switching circuit coupled to the scan-path interface. The Examiner states that Raghavavhari discloses that many integrated circuits are access via scan-ports and specifically discloses a switching circuit coupled to the scan-path interface. The Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Palmer, Jr. et al with Raghavavhari.

Assuming, arguendo, that Palmer, Jr. et al and Raghavavhari were to be combined, this still would not teach the utilization of applying commands to a plurality of ports to be processed into a password because Raghavavhari only shows a single input port and Palmer, Jr. et al., which does show two input ports, shows them being used each for separate purposes. Accordingly, even if these two devices could be combined, it would not yield the present invention or suggest the present invention.

The Examiner states with regard to Claims 5 and 10, the Palmer, Jr. et al reference inherently discloses a specified time sequence.

The "sequence" of Palmer, Jr. et al would that the input through main computer interface 6a would have to occur at a time previous to the input to card reader 4, 6c. However, the reference fails to show or suggest the application of a plurality of commands applied to a plurality of input ports in a specific time sequence to be processed into a password, as would be required by the combination of Claims 4, 5 and 8, 10, respectively.

The Examiner rejects Claims 6, 7, 11, 12, 13, 16, 17, 19, 20 and 21 under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al in view of Raghavavhari and further in view of Jacobson, et al. These claims are dependent upon Claims 4, 8 or 14, the patentability of which has been discussed above. These claims are patentable for the same reasons.

The Examiner rejects Claim 18 under 35 U.S.C. 103(a) as being unpatentable over Palmer, Jr. et al in view of Jacobson, et al. Claim 18 is dependent upon Claim 14. The patentability of Claim 14 over the Palmer, Jr. et al reference having been discussed above, Claim 18 is patentable for the same reasons.

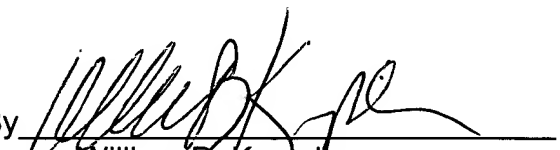
The Examiner rejects Claims 4-13, and 16-21 under U.S.C. 103(a) as being unpatentable over Angelo over Bianco, et al. The Examiner states that Angelo discloses a method for enabling power to all or portions of a computer system based on the results of a 2-piece user verification process that is completed as part of a secure power-up procedure. The Examiner states that Angelo does not expressly disclose a scan-pass interface circuit for comparison for a predetermined memory or register and a switching circuit is responsive to the comparison. The Examiner states that Bianco, et al. discloses a set/scan test capability which is provided for a circuit that includes sensitive subcircuits that can be latched out to prevent reverse engineering of the sensitive elements. The Examiner states that various implementations are possible, such as fusable-link PROMs for irreversibly inhibiting set/scan access to the sensitive subcircuits, the use of encryption codes to enable repeated set/scan access to the sensitive subcircuits and that erasable/reprogrammable mechanism for inhibiting set/scan access. The Examiner concludes that it would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the Angelo reference with Bianco, et al. reference.

This rejection is respectfully traversed. The Angelo reference has been discussed above in connection with the rejection of Claims 14 and 15. As stated above, Angelo specifically shows all of the inputs needed to generate the password coming

through a single input port to the processor. With respect to Bianco, et al, the Examiner specifically points to Figure 6. Figure 6 does show a CPU connected to a system to protect sensitive information from a data scan. However, reading the remainder of the reference, it is clear the protection is provided by an encryption program stored in EEPROM 58. Once the device has been tested by the manufacturer, the system is programmed to bypass the data stored in the sensitive area unless a code equal to that stored in the EEPROM is applied. There is nothing in this reference that shows or even suggests the application of a plurality of commands to a plurality of ports for the processor 50 to be processed into a password. The password goes through the S/S control 14. Furthermore, the system of Bianco, et al requires considerable additional circuitry to that of the present invention. In fact, the elegance of the present invention is that no additional circuitry is required, it utilizes attributes of the microprocessor that are already present to provide the additional security. Therefore, this reference singly, or in combination Angelo does not show or suggest the present invention. Accordingly, the present claims already clearly distinguished from these references either singly or in combination.

Accordingly, applicants believe the application, as amended is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
Texas Instruments Incorporated

By 

William B. Kempler
Senior Corporate Patent Counsel
Reg. No. 28,228
Tel.: (972) 917-5452

Attachments